

What is claimed is:

## CLAIMS

1. An SATA (Serial AT Attachment) host controller capable of performing  
5 host-to-device and device-to-host communications, the host controller being  
operable in a PIO (Programmed I/O) data transfer mode and a DMA (Direct  
Memory Access) data transfer mode, the host controller comprising:  
  
a buffer unit for buffering data; and  
  
a data stream selection unit for selecting a data stream for submission to said  
10 buffer unit,  
  
wherein the data stream selection unit is connected to receive at any one time  
at least one of a host-to-device data stream in the PIO data transfer mode, a  
host-to-device data stream in the DMA data transfer mode, a device-to-host  
data stream in the PIO data transfer mode, and a device-to-host data stream in  
15 the DMA data transfer mode, and select from said received data streams the  
data stream to be submitted to said buffer unit.
2. The SATA host controller of claim 1, further comprising:  
  
a bus master engine for performing host-to-device and device-to-host  
communications in the DMA data transfer mode by accessing host memory,  
  
20 wherein said bus master engine is connected to said buffer unit for receiving  
said device-to-host data stream in the DMA data transfer mode, and to said  
data stream selection unit for providing said host-to-device data stream in said  
DMA data transfer mode.
3. The SATA host controller of claim 2, wherein said bus master engine is  
25 arranged to support at least five outstanding read requests.

4. The SATA host controller of claim 2, wherein said bus master engine is arranged to request bursts with the maximum burst length in response to physical region descriptors.
5. The SATA host controller of claim 2, wherein said buffer unit is arranged to  
5 provide a first status signal to said bus master engine when performing device-to-host communications, said first status signal indicating that the current buffer fill level is equal to or above a first predefined fill level.
6. The SATA host controller of claim 5, wherein said buffer unit is further arranged to provide a second status signal to said bus master engine when  
10 performing device-to-host communications, said second status signal indicating the current fill level is equal to or below a second predefined fill level.
7. The SATA host controller of claim 6, wherein said second predefined fill level is lower than said first predefined fill level.
8. The SATA host controller of claim 6, wherein said first predefined fill level  
15 defines free buffer capacity of 44 double words.
9. The SATA host controller of claim 6, wherein said second predefined fill level defines free buffer capacity of 48 double words.
10. The SATA host controller of claim 1, further comprising:  
a target interface unit for performing host-to-device and device-to-host  
20 communications in the PIO data transfer mode,  
wherein said target interface unit is connected to said buffer unit for receiving said device-to-host data stream in the PIO data transfer mode, and to said data stream selection unit for providing said host-to-device data stream in said PIO data transfer mode.
- 25 11. The SATA host controller of claim 1, further comprising:  
an SATA controller unit for controlling data transfer to and from a physical interface unit,

wherein said SATA controller unit is connected to said buffer unit for receiving host-to-device data, and to said data stream selection unit for providing device-to-host data, in both the DMA and the PIO data transfer modes.

12. The SATA host controller of claim 1, wherein said buffer unit is arranged to  
5 have a buffer capacity of six or more cachelines when buffering data relating to host-to-device communications in the DMA data transfer mode.
13. The SATA host controller of claim 1, wherein said buffer unit is arranged to have a buffer capacity of five or more cachelines when buffering data relating to device-to-host communications in the DMA data transfer mode.
- 10 14. The SATA host controller of claim 1, wherein said buffer unit is arranged to have a buffer capacity of two 32-bit registers when buffering data relating to host-to-device communications in the PIO data transfer mode.
- 15 15. The SATA host controller of claim 1, wherein said buffer unit is arranged to have a buffer capacity of at least 45 double words when buffering data relating to device-to-host communications in the PIO data transfer mode.
16. The SATA host controller of claim 1, wherein said buffer unit is operable in a FIFO (First In First Out) mode for writing data to said buffer unit.
17. The SATA host controller of claim 1, wherein said buffer unit is operable in a FIFO (First In First Out) mode for reading data from said buffer unit.
- 20 18. The SATA host controller of claim 1, wherein said buffer unit is operable in a direct addressing mode for writing data to said buffer unit.
19. The SATA host controller of claim 18, wherein said buffer unit is operable in said direct addressing mode for writing data of said host-to-device data stream in the direct memory access data transfer mode to said buffer unit.
- 25 20. The SATA host controller of claim 1, wherein said buffer unit is controlled to output read responses pertaining to said host-to-device data stream in the direct memory access data transfer mode, in a reordered sequence.

21. The SATA host controller of claim 1, wherein said buffer unit comprises a first two-port RAM (Random Access Memory) device and a second two-port RAM device.
22. The SATA host controller of claim 1, wherein said data stream selection  
5 unit is a multiplexer unit.
23. The SATA host controller of claim 1, wherein said DMA data transfer mode is a UDMA (Ultra DMA) data transfer mode.
24. A storage device host controller capable of performing host-to-device and device-to-host communications, the host controller being operable in a  
10 programmed input/output data transfer mode and a direct memory access data transfer mode, the host controller comprising:
- a buffer unit for buffering data; and
- a data stream selection unit for selecting a data stream for submission to said buffer unit,
- 15 wherein said data stream selection unit is connected to receive at any one time at least one of a host-to-device data stream in the programmed input/output data transfer mode, a host-to-device data stream in the direct memory access data transfer mode, a device-to-host data stream in the programmed input/output data transfer mode, and a device-to-host data stream in the direct  
20 memory access data transfer mode, and select from said received data streams the data stream to be submitted to said buffer unit.
25. An integrated circuit chip for performing host-to-device and device-to-host ATA (AT Attachment) communications in a PIO (Programmed I/O) data transfer mode and a DMA (Direct Memory Access) data transfer mode, the integrated  
25 circuit chip comprising:
- a buffer circuit for buffering data; and

a data stream selection circuit for selecting a data stream for submission to said buffer circuit,

wherein said data stream selection circuit is connected to receive at any one time at least one of a host-to-device data stream in the PIO data transfer mode,  
5 a host-to-device data stream in the DMA data transfer mode, a device-to-host data stream in the PIO data transfer mode, and a device-to-host data stream in the DMA data transfer mode, and select from said received data streams the data stream to be submitted to the buffer circuit.

26. A method of operating an SATA (Serial ATA) host controller to perform  
10 host-to-device and device-to-host communications in a PIO (Programmed I/O) data transfer mode, and a DMA (Direct Memory Access) data transfer mode, comprising:

receiving at any one time at least one of a host-to-device data stream in the PIO data transfer mode, a host-to-device data stream in the DMA data transfer  
15 mode, a device-to-host data stream in the PIO data transfer mode, and a device-to-host data stream in the DMA data transfer mode;

selecting from said received data streams a data stream to be buffered; and

buffering data of the selected data stream in a buffer unit.

27. The method of claim 26, further comprising the step of:

20 operating a bus master engine for performing host-to-device and device-to-host communications in the DMA data transfer mode by accessing host memory, said step of operating the bus master engine comprising:

receiving said device-to-host data stream in the DMA data transfer mode from said buffer unit; and

25 providing said host-to-device data stream in said DMA data transfer mode to be selected.

28. The method of claim 27, wherein said step of operating the bus master engine is arranged to support at least five outstanding read requests.

29. The method of claim 27, wherein said step of operating the bus master engine comprises:

- 5 requesting bursts with the maximum burst length in response to physical region descriptors.

30. The method of claim 27, wherein the step of buffering data comprises:

- providing a first status signal to said bus master engine when performing device-to-host communications, said first status signal indicating that the current  
10 buffer fill level of the buffer unit is equal to or above a predefined fill level.

31. The method of claim 30, wherein said step of buffering data further comprises:

- providing a second status signal to said bus master engine when performing device-to-host communications, said second step signal indicating that the  
15 current fill level is equal to or below a second predefined fill level.

32. The method of claim 31, wherein said second predefined fill level is lower than said first predefined fill level.

33. The method of claim 31, wherein said first predefined fill level defines free buffer capacity of 44 double words.

- 20 34. The method of claim 31, wherein said second predefined fill level defines free buffer capacity of 48 double words.

35. The method of claim 26, further comprising;

- operating a target interface unit for performing host-to-device and device-to-host communications in the PIO data transfer mode, the step of operating the target  
25 interface unit comprising:

receiving said device-to-host data stream in the PIO data transfer mode from said buffer unit; and

providing said host-to-device data stream in said PIO data transfer mode.

36. The method of claim 26, further comprising:

- 5 controlling data transfer to and from a physical interface unit in an SATA controller unit, said SATA controller unit being operated by receiving host-to-device data from said buffer unit and providing device-to-host data to be selected, in both the DMA and the PIO data transfer modes.

37. The method of claim 26, wherein said step of buffering data comprises  
10 buffering six or more cachelines when performing host-to-device communications in the DMA data transfer mode.

38. The method of claim 26 wherein said step of buffering data comprises buffering five or more cachelines when performing device-to-host communications in the DMA data transfer mode.

15 39. The method of claim 26, wherein the step of buffering data comprises operating two 32-bit registers when buffering data relating to the host-to-device communications in the PIO data transfer mode.

40. The method of claim 26, wherein the step of buffering data comprises buffering at least 45 double words when performing device-to-host  
20 communications in the PIO data transfer mode.

41. The method of claim 26, wherein the step of buffering data comprises:

operating said buffer unit in a FIFO (First In First Out) mode for writing data to said buffer unit.

42. The method of claim 26, wherein buffering data comprises:

25 operating said buffer unit in a FIFO (First In First Out) mode for reading data from said buffer unit.

43. The method of claim 26, wherein buffering data comprises:

operating said buffer unit in a direct addressing mode for writing data to said buffer unit.

44. The method of claim 43, wherein said buffer unit is operable in said direct  
5 addressing mode for writing data of said host-to-device data stream in the direct memory access data transfer mode to said buffer unit.

45. The method of claim 26, further comprising:

outputting buffered read responses pertaining to said host-to-device data  
stream in the direct memory access data transfer mode, in a reordered  
10 sequence.

46. The method of claim 26, wherein buffering data comprises:

operating a first two-port RAM (Random Access Memory) device; and

operating a second two-port RAM device.

47. The method of claim 26, wherein said step of selecting a data stream  
15 comprises multiplexing the received data streams.

48. The method of claim 26, wherein said DMA data transfer mode is a UDMA  
(Ultra DMA) data transfer mode.

49. A method of operating a storage device host controller to perform host-to-  
device and device-to-host communications in a programmed input/output data  
20 transfer mode and a direct memory access data transfer mode, the method comprising:

receiving at any one time at least one of a host-to-device data stream in the  
programmed input/output data transfer mode, a host-to-device data stream in  
the direct memory data transfer mode, a device-to-host data stream in the  
25 programmed input/output data transfer mode, and a device-to-host data stream  
in the direct memory access data transfer mode;



selecting from said received data streams a data stream to be buffered; and

buffering data of the selected data stream in a buffer unit.